Constant and Switched Bias Low Frequency Noise in p-MOSFETs with Varying Gate Oxide Thickness

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Abstract

The low-frequency noise power spectral density of MOSFETs is decreased if the MOSFETs are periodically switched 'off' (switched bias conditions). The influence of the gate oxide thickness on fixed bias and switched biased low frequency drain current noise spectral density of PMOS devices has been experimentally investigated. Under constant bias conditions, it is observed that the current noise spectral density increases linearly with increase in the gate oxide thickness. The larger the measured low-frequency noise under constant bias, the larger is the noise reduction after periodically switching the P-MOSFETs off.

1. Introduction

The low-frequency noise in MOSFETs increases with shrinking device dimensions. Thus it becomes increasingly important when designing analog and RF applications in modern CMOS technologies. The two main theories which explain the low-frequency or 1/f noise behavior in MOSFETs are based on the mobility fluctuation model described by the Hooge parameter and the number fluctuation model based on the theory of trapping and detrapping of charge carriers in traps located in the oxide or at the interface [1]-[3]. The Unified model for the flicker noise proposed by Hung et al. [4], incorporates both the number fluctuations and the surface mobility fluctuations. Previously, it had been reported, that the noise power spectral density of the low frequency noise of MOSFETs decreases, if the transistors are switched "off" periodically [5]-[7].

A noise reduction of 6 dB is expected, with a 50% duty cycle of the switching pulse. But the measurement results show a noise reduction of more than 6 dB [6], [7]. The gate oxide thickness dependence on the low-frequency noise of MOSFETs has been reported previously [8]. In this work, we report the constant bias low-frequency noise measurements and also the switched biased noise measurements on p-MOSFETs with varying gate oxide thickness.

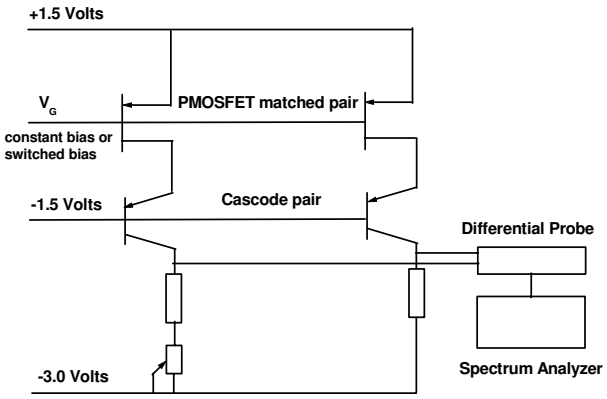

Figure 1. Circuit diagram for constant DC biased and switched biased noise measurements

2. P-MOSFET Noise Measurements

The wafers on which the p-MOSFET noise measurements are carried out have a substrate doping of $5\times10^{17}cm^{-3}$, and a gate oxide thickness of 2.0; 3.6; 7.5; 10 or 20nm. The noise measurements are carried out on transistors with geometry W:L=10:1 and 10:0.3 (W and L are the width and length of the p-MOSFET in μm). The noise measurement set up used is functionally similar to the one used by van der Wel et al. [6], with NPN transistors replaced by PNP transistors. Figure 1. shows the circuit used for the noise measurements. The p-MOSFETs on the wafer are a matched pair (identical in geometry and all electrical properties). A differential probe is used to cancel out the common mode signals. The set up keeps the drain voltages of the matched pair of p-MOSFET, almost constant. The differential drain current is converted into an equivalent voltage, whose spectral density is then measured by a spectrum analyzer. The noise measurement set up measures the drain current noise spectral density (S_{ID}) of the p-MOSFET. The switched bias voltage is applied to the gate of the p-MOSFET to periodically switch the transistors "off". Thus, in this manner the constant bias noise spectrum

and switched bias noise spectrum are obtained. A constant drain current of 17 µA is forced through the p-MOSFETs, during each of the constant DC bias measurements. The $|V_{GS}-V_T|$ value is kept at around 0.4 volts, ensuring that the p-MOSFETs are in the saturation region, and also in strong inversion. The "off" gate bias voltage is then varied from, just below the threshold voltage to well below the threshold voltage, and the corresponding switched bias noise is measured.

3. Measurement Results

Figure 2. shows the noise power spectral density of a p-channel MOSFET with geometry W:L=10:0.3 and gate oxide thickness of 20nm, under constant bias conditions and under switched bias conditions. A noise reduction of more than 6 dB is observed, when the transistors are periodically switched 'off'. The low-frequency noise is measured on the linear portion of the noise spectrum at around 100Hz. The noise reduction is the difference between the constant bias low-frequency noise and the noise measured when the gates of the p-MOSFET are periodically switched on and off.

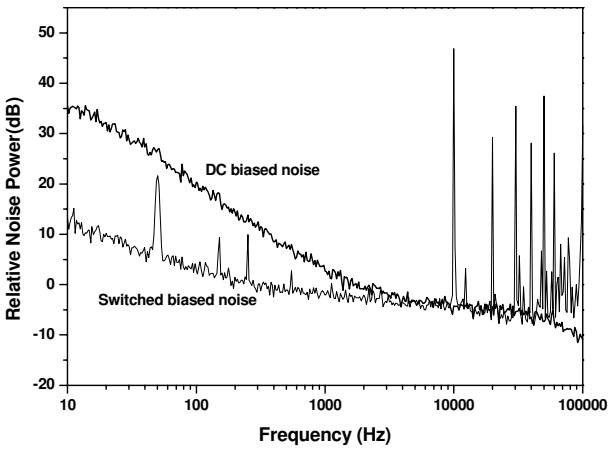

Figure 2. Noise spectral density constant biased gate and switched biased gate. t_{OX}=20nm, W:L=10:0.3, $V_{GS}-V_T$=0.4V, I_{DS}=17µA

Figure 3. shows the noise reduction obtained as a function of the 'off' value of the (switching) gate voltage. Also shown is the expected noise reduction, which is 6 db below the DC biased value, because of the 50% duty cycle of the switching gate signal [6]. The noise reduction increases with increase in the 'off' value (beyond threshold) and then finally tends to saturate, suggesting a limit to the amount of noise reduction that can be obtained as a result of 'switched bias'. In Fig. 4, the drain current noise spectral density for different gate oxide thickness is shown under constant bias conditions (constant $|V_{GS}-V_T|$). The low-frequency noise is then plotted as a function of the gate oxide thickness (t_{ox}) in Fig. 5. The data points show a power dependence on t_{ox}, with the power 'p' close to unity.

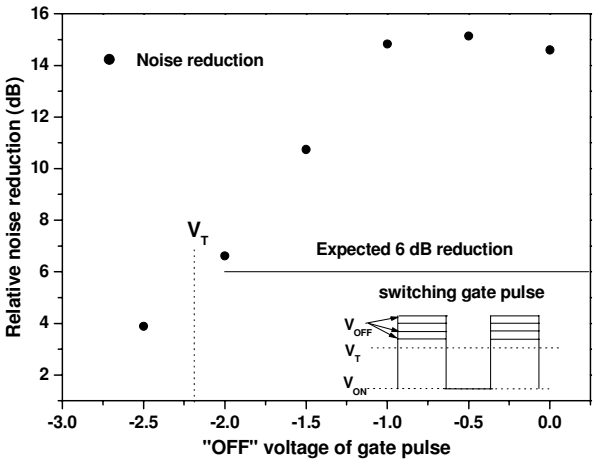

Figure 3. Noise reduction as a function of the "off" voltage of the gate pulse. Also shown is the expected 6 dB reduction for a 50% duty cycle of gate pulse

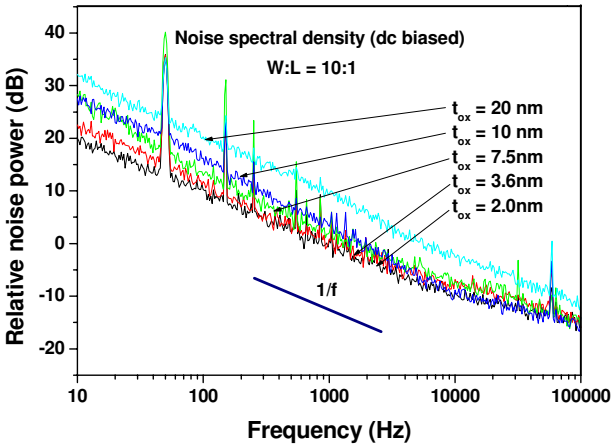

Figure 4. Noise spectral density of p-MOSFETs with W:L=10:1, and I_{DS}=17µA

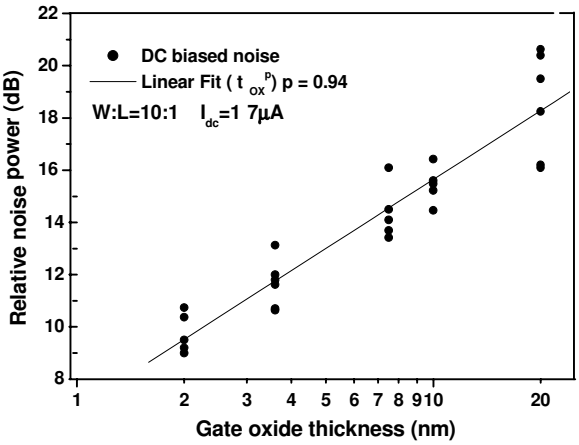

Figure 5. S_{ID} versus t_{ox} for PMOS devices with W:L=10:1

The noise measurements on p-MOSFETs with smaller geometry (W:L=10:0.3), shows that there is a larger variation from sample to sample as compared to devices with larger geometry (W:L=10:1). The constant bias noise measurements and switched bias noise measurements are done on different PMOS transistors with similar geometry (W/L=10/0.3) and varying t_{ox}. During the switched bias noise measurements on devices with different t_{ox}, the amplitude of the switching gate voltage is kept constant. The 'off' voltage of the switching gate voltage is kept in the region where the maximum possible noise reduction is observed.

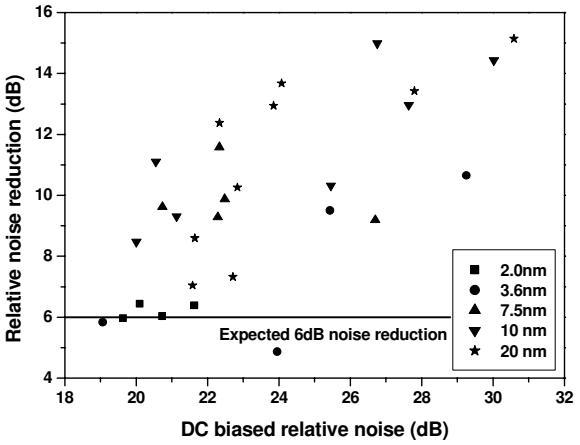

Figure 6. Noise reduction obtained by switched bias against the constant bias noise, for different PMOS devices with different t_{ox} (W:L=10:0.3)

Figure 6. shows the noise reduction obtained in each case (during switched bias) as against the low-frequency noise measured (under constant bias), for devices with different t_{ox}. The number of points is the number of PMOS devices measured. The larger the low-frequency noise under constant bias, the larger was the noise reduction obtained on that transistor when subjected to switched bias conditions.

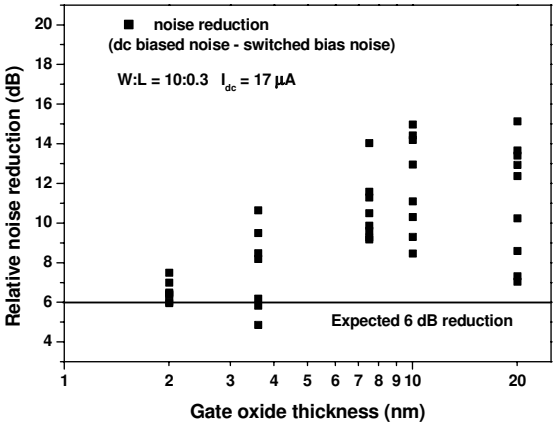

Figure 7. Noise reduction obtained after switched bias versus the gate oxide thickness for different PMOS devices (W:L=10:0.3)

In Fig. 7, the noise reduction obtained for each device is plotted against the gate oxide thickness. In each of the measurements, the switching amplitude (switched bias case) and the drain current (constant bias case) is kept constant. As seen from the figure, the noise reduction increases as the gate oxide thickness increases. This can be explained from Fig. 5, and Fig. 6. The constant or DC biased noise increases as the gate oxide thickness increases, and the noise reduction is larger when the constant biased noise is large. Thus combining these two results, we expect a larger noise reduction for devices with thicker t_{ox}. A similar trend is observed for transistors with geometry 10:1. Note that for almost all the devices the noise reduction measured was greater than 6 dB, the expected noise reduction for a 50% duty cycle of gate voltage.

4. Discussions

The switched biased noise measurement results can be explained qualitatively as follows. The low frequency noise in the p-MOSFETs can be explained by the number fluctuation theory based on the theory of trapping and de-trapping of mobile charge carriers in traps located at the silicon interface and in the oxide. When a transistor is periodically switched "off", there is a high probability that the traps with energies located close to the Fermi level, are emptied. The mean values of the capture time (τ_c) and the emission time (τ_e) of the trap are now changed. Thus the periodic switching of the gate voltage forces the traps near the Fermi level to be in either the empty or filled state. This in turn leads to a reduced noise spectrum at low frequencies.

The models available in literature [1]-[4] for explaining the low-frequency noise are the mobility fluctuation model and the number fluctuation model. S_{Vgate}, the noise spectral density referred to the gate side, is given by $S_{Vgate} = S_{ID}/(g_m)^2$, where S_{ID} is the drain current noise spectral density and g_m is the MOSFET transconductance. The mobility fluctuation model predicts a linear t_{ox} dependence on S_{Vgate}, where as the number fluctuation model predicts a t_{ox}^2 dependence on S_{Vgate}. Our p-MOSFET measurement results show a t_{ox} dependence on S_{ID} and thus t_{ox}^2 dependence on S_{Vgate}. This indicates that the number fluctuation model describes our p-MOSFETs better than the mobility fluctuation model. This, coupled with the switched biased noise measurement results, gives a strong indication that the physical origin of low-frequency noise in p-MOSFETs with smaller geometry is due to the random trapping and de-trapping of charge carriers in the traps located in the oxide or at the interface.

5. Conclusions

The influence of gate oxide thickness (t_{ox}) on p-MOSFETs low-frequency noise, under constant bias and switched bias, has been investigated for the first time. A

linear t_{ox} dependence on S_{ID} (constant bias drain current spectral noise density), and the fact that we get a noise reduction after switched biasing the gate, suggests that the source of origin for the low-frequency noise is due to the random trapping and de-trapping of charge carriers in the traps located in the oxide or at the interface. In almost all cases, the low-frequency noise reduction obtained for the p-MOSFETs, was more than 6 dB. The larger the low-frequency noise in a p-MOSFET, the larger was the noise reduction measured under switched bias conditions.

6. Acknowledgments

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7. References

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